CLAIMS

What is claimed is:

Sub A1

1. An integrated circuit comprising:

a memory array, wherein the memory array is divided into m partitions, wherein m is an integer greater than or equal to two;

a microcontroller coupled to a status register, wherein the status register reports status information of m memory partitions.

2. The integrated circuit of claim 1, wherein the memory array is coupled to the status register by a decoder circuit.

3. The integrated circuit of claim 1, further comprising:

the microcontroller coupled to a logic block;

the logic block coupled to the status register;

the status register coupled to a user interface.

4. The integrated circuit of claim 3, further comprising:

the user interface coupled to an address latch;

the address latch coupled to the logic block.

5. The integrated circuit of claim 3, wherein the user interface communicates status register information to be used to decide subsequent operations.

6. A method of reading while writing to a memory array, comprising:

dividing the memory array into n planes, wherein n is an integer greater than or equal to two;

defining a write partition, wherein the write partition is a single plane of the memory array;

defining a read partition, wherein the read partition is made up of all of the

remaining n planes of the memory array;

providing the status of the read partition and the write partition of the memory array with a single status register.

7. The method of claim 6, wherein the memory array consists of multiple 4 Mb memory planes.

8. The method of claim 7, wherein the multiple 4 Mb memory planes consist of nonvolatile memory cells.

9. The method of claim 8, wherein the nonvolatile memory cell is a flash memory cell.

10. The method of claim 7, wherein the write partition has a dynamic memory address, wherein the memory address changes any time a program or erase operation begins or resumes in a new memory plane.

11. The method of claim 7, wherein if no program or erase operation is performed, the read partition and the write partition are allocated to the same memory location.

12. A method of operating a status register, comprising:

receiving a plane memory address and signals from the user interface;

latching a plane memory address whenever a write operation is beginning or resuming;

evaluating the current command plane address with the previous plane memory address;

outputting status bits to the user interface.

13. The method of claim 12, wherein a comparator is used to evaluate the current command plane address with the previous plane memory address.

14. The method of claim 12, wherein the output status bits comprise:

a device write status bit, wherein the device write status provides the status of the block erase or program completion in the device;

a partition write status bit, wherein the partition write status provides the block erase or program executions in the current plane.

15. The method of claim 14, wherein the output status bits further comprise:

an erase suspend status bit;

an erase status bit;

a program status bit;

a voltage status bit;

a program suspend status bit;

a device protect status bit.

16. The method of claim 14, wherein the device write status bit and the partition write status bit are not busy at the same time.

17. The method of claim 15, wherein the program status bit is a logical OR of the information of each of the m partitions, the erase status bit is a logical OR of the information of each of the m partitions, the program status suspend bit is a logical OR of the information of each of the m partitions, and the erase status suspend bit is a logical OR of the information of each of the m partitions.

18. An apparatus comprising:

means for partitioning a memory array to enable multiple operations to be performed on the memory array at the same time; and

means for monitoring the operations performed on the memory array.

19. The apparatus of claim 18 further comprising a means for communicating the status of the operations performed on the memory array to a user.